

Substitute the following set of claims, which included the amended claims and the claims which were not amended, on pages 29-44:

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1. A multipath-combining subsystem for use with a spread-spectrum receiver for receiving a spread-spectrum signal arriving at different times from a plurality of paths, with the spread-spectrum signal having a plurality of packets with each packet having a header followed by a data portion, with the header including a header-chip-sequence signal, and with the data portion including a data-symbol-sequence signal, with each data symbol of the data-symbol-sequence signal spread-spectrum processed by a data-chip-sequence signal, said multipath-combining subsystem comprising:

matched-filter means, coupled to said spread-spectrum receiver, having a first impulse response matched to the header-chip-sequence signal of the header embedded in the spread-spectrum signal, for detecting, within a packet and for each path of the spread-spectrum signal, each match of the header-chip-sequence signal with the first impulse response, with a time difference between receiving each path of the spread-spectrum signal greater than a time of each chip of the header-chip-sequence signal and greater than a time of each chip of the data-chip-sequence signal, and for outputting, responsive to a detected match having a correspondence between the header-chip-sequence signal and the first impulse response above a header

threshold, a header detection signal having an in-phase-header amplitude and a quadrature-phase-header amplitude and a respective chip location;

header-memory means, coupled to said matched-filter means, for storing the in-phase-header amplitude and the quadrature-phase-header amplitude of each header-detection signal and the respective chip location of each header-detection signal;

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and.  
said matched-filter means having a second impulse response matched to the data-chip-sequence signal of the data portion embedded in the spread-spectrum signal, for detecting, at the respective chip location of each header-detection signal for each path, each match of the data-chip-sequence signal with the second impulse response, and for outputting, responsive to each detected match, a data-detection signal having an in-phase-data amplitude and a quadrature-phase data amplitude; and

combining means, coupled to said header-memory means and to said matched-filter means, for multiplying the in-phase-header amplitude and the quadrature-phase-header amplitude of each header-detection signal by the in-phase-data amplitude and the quadrature-phase-data amplitude of each data-detection signal at each corresponding chip location, respectively, thereby generating a plurality of in-phase-weighted elements and a plurality of quadrature-phase-weighted elements for each data symbol within the data portion, and for combining the plurality of in-phase-weighted elements and the plurality of quadrature-

phase-weighted elements of a respective data symbol as a sum signal of the respective data symbol.

2. The multipath-combining subsystem as set forth in claim 1 wherein said combining means includes:

product means for multiplying the in-phase-header amplitude and the quadrature-phase-header amplitude of each header-detection signal by the in-phase-data amplitude and the quadrature-phase-data amplitude of each data-detection signal, at each corresponding chip location, respectively, thereby generating the plurality of in-phase-weighted elements and the plurality of quadrature-phase-weighted elements for each data symbol of the data-symbol-sequence signal;

a combiner memory for storing the plurality of in-phase-weighted elements and the plurality of quadrature-phase-weighted elements; and

adding means for adding each in-phase-weighted element of the plurality of in-phase-weighted elements, and for adding each quadrature-phase-weighted element of the plurality of quadrature-phase-weighted elements for each data symbol to generate the sum signal of the respective data symbol.

3. The multipath-combining subsystem as set forth in claim 1 further including:

a header-pattern generator, responsive to the header-detection signal, for generating a header pattern; and

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said matched-filter means, responsive to the header pattern, for detecting each match of the data-chip-sequence signal with the second impulse response.

4. The multipath-combining subsystem as set forth in claim 3 wherein said combining means includes:

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product means for multiplying the in-phase-header amplitude and the quadrature-phase-header amplitude of each header-detection signal by the in-phase-data amplitude and the quadrature-phase-data amplitude of each data-detection signal, at each corresponding chip location, respectively, thereby generating the plurality of in-phase-weighted elements and the plurality of quadrature-phase-weighted elements for each data symbol of the data-symbol-sequence signal;

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a combiner memory for storing the plurality of in-phase-weighted elements and the plurality of quadrature-phase-weighted elements; and

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adding means for adding each in-phase-weighted element of the plurality of in-phase-weighted elements, and for adding each quadrature-phase-weighted element of the plurality of quadrature-phase-weighted elements for each data symbol to generate the sum signal of the respective data symbol.

5. The multipath-combining subsystem as set forth in claim 1 further including a demodulator, coupled to said combining means, for detecting data from the sum signal.

6. The multipath-combining subsystem as set forth in claim 1 further including:

a header-timing circuit for detecting, from a plurality of header-detection signals, a strongest header-detection signal and, responsive to the strongest header-detection signal, for outputting a packet-start signal; and

said matched-filter means, responsive to the packet-start signal, for changing the first impulse response to the second impulse response.

7. The multipath-combining subsystem as set forth in claim 1 wherein said matched-filter means includes:

a header-matched filter, coupled to said spread-spectrum receiver, having the first impulse response matched to the header-chip-sequence signal of the header embedded in the spread-spectrum signal, for detecting, within each packet and for each path of the spread-spectrum signal, each match of the header-chip-sequence signal with the first impulse response, and for outputting, responsive to a detected match having a level of correspondence above the header threshold, the header-detection signal having the in-phase-header amplitude and the quadrature-phase-header amplitude and a respective chip location; and

a data-matched filter, having the second impulse response matched to the data-chip-sequence signal of the data portion embedded in the spread-spectrum signal, for detecting, at the respective chip location of each header-detection signal

for each path, each match of the data-chip-sequence signal with the second impulse response, and for outputting, responsive to each detected match, the in-phase-data amplitude and the quadrature-phase-data amplitude of the data-detection signal.

8. The multipath-combining subsystem as set forth in claim 1 wherein said matched-filter means includes:

15 a programmable-matched filter, coupled to said spread-spectrum receiver, having the first impulse response initially matched to the header-chip-sequence signal of the header embedded in the spread-spectrum signal, for detecting, within each packet and for each path of the spread-spectrum signal, each match of the header-chip-sequence signal with the first impulse response, and for outputting, responsive to a detected match having a level of correspondence above the header threshold, a header detection signal having the in-phase-header amplitude and the quadrature-phase-header amplitude and a respective chip location; and

15 said programmable-matched filter, having the second impulse response matched to the data-chip-sequence signal of the data portion embedded in the spread-spectrum signal, for detecting, at the respective chip location of each header-detection signal for each path, each match of the data-chip-sequence signal with the second impulse response, and for outputting, responsive to each detected match, the in-phase-data amplitude and the quadrature-phase-date amplitude of the data-

detection signal.

9. The multipath-combining subsystem as set forth in claim 7 ~~or 8~~ wherein said combining means includes:

product means for multiplying the header amplitude of each header-detection signal by the data amplitude of each data-detection signal, at each corresponding chip location, respectively, thereby generating the plurality of in-phase-weighted elements and the plurality of quadrature-phase-weighted elements for each data symbol of the data-symbol-sequence signal;

a combiner memory for storing the plurality of in-phase-weighted elements and the plurality of quadrature-phase-weighted elements; and

adding means for adding each in-phase-weighted element of the plurality of in-phase-weighted elements, and for adding each quadrature-phase-weighted element of the plurality of quadrature-phase-weighted elements for each data symbol to generate the sum signal of the respective data symbol.

10. A multipath-combining subsystem for use with a spread-spectrum receiver for receiving a spread-spectrum signal arriving at different times from a plurality of paths, with the spread-spectrum signal having a plurality of packets with each packet having a header followed by a data portion, with the header including a header-chip-sequence signal, and with the

data portion including a data-symbol-sequence signal, with each data symbol of the data-symbol-sequence signal spread-spectrum processed by a data-chip-sequence signal, said multipath-combining subsystem comprising:

10 a header-matched filter, coupled to said spread-spectrum receiver, having a first impulse response matched to the header-chip-sequence signal of the header embedded in the spread-spectrum signal, for detecting, within a packet and for each path of the spread-spectrum signal, each match of the header-chip-sequence signal with the first impulse response, with a time difference between receiving each path of the spread-spectrum signal greater than a time of each chip of the header-chip-sequence signal and greater than a time of each chip of the data-chip-sequence signal, and for outputting, responsive to a detected match having a correspondence between the header-chip-sequence signal and the first impulse response above a header threshold, a header detection signal having an in-phase header amplitude and a quadrature-phase-header amplitude and a respective chip location;

20 a header memory, coupled to said header-matched filter, for storing the in-phase-header amplitude and the quadrature-phase-header amplitude of each header-detection signal and the respective chip location of each header-detection signal;

25 a symbol-matched filter, having a second impulse response matched to the data-chip-sequence signal of the data



portion embedded in the spread-spectrum signal, for detecting,  
at the respective chip location of each header-detection signal  
for each path, each match of the data-chip-sequence signal with  
the second impulse response, and for outputting, responsive to  
each detected match, a data-detection signal having an in-phase-  
data amplitude and a quadrature-phase data amplitude;

40 a header-timing circuit, coupled to an output of said  
header-matched filter, for detecting, from a plurality of  
header-detection signals, a strongest header-detection signal  
and, responsive to the strongest header-detection signal, for  
outputting a packet-start signal;

45 product means, coupled to an output of said header-  
matched filter and to an output of said header-timing circuit,  
for multiplying the in-phase-header amplitude and the  
quadrature-phase-header amplitude of each header-detection  
signal by the in-phase-data amplitude and the quadrature-phase-  
data amplitude of each data-detection signal, at each  
50 corresponding chip location, respectively, thereby generating  
the plurality of in-phase-weighted elements and the plurality of  
quadrature-phase-weighted elements for each data symbol of the  
data-symbol-sequence signal;

55 adding means, coupled to an output of said product  
means, for adding the plurality of in-phase-weighted elements  
and the plurality of quadrature-phase-weighted elements for a  
respective data symbol to generate a sum signal of the  
respective data symbol;

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a combiner memory, coupled to an output of said adding means, for storing the sum signal; and

a data demodulator, coupled to said combiner memory, for detecting data from the sum signal.

11. A multipath-combining subsystem for use with a spread-spectrum receiver for receiving a spread-spectrum signal arriving at different times from a plurality of paths, with the spread-spectrum signal having a plurality of packets with each packet having a header followed by a data portion, with the header including a header-chip-sequence signal, and with the data portion including a data-symbol-sequence signal, with each data symbol of the data-symbol-sequence signal spread-spectrum processed by a data-chip-sequence signal, said multipath-combining subsystem comprising:

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a programmable-matched filter, coupled to said spread-spectrum receiver, having a first impulse response matched to the header-chip-sequence signal of the header embedded in the spread-spectrum signal, for detecting, within a packet and for each path of the spread-spectrum signal, each match of the header-chip-sequence signal with the first impulse response, with a time difference between receiving each path of the spread-spectrum signal greater than a time of each chip of the header-chip-sequence signal and greater than a time of each chip of the data-chip-sequence signal, and for outputting, responsive to each detected match above a header threshold, an in-phase-

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header amplitude and a quadrature-phase-header amplitude and a respective chip location;

25 a header memory, coupled to said programmable-matched filter, for storing the in-phase-header amplitude and the quadrature-phase-header amplitude and the respective chip location of each header-detection signal;

30 a header-timing circuit, coupled to an output of said programmable-matched filter, for detecting, from a plurality of header-detection signals, a strongest header-detection signal and, responsive to the strongest header-detection signal, for outputting a packet-start signal;

35 said programmable-matched filter, responsive to the packet-start signal, for changing the first impulse response to a second impulse response, the second impulse response matched to the data-chip-sequence signal of the data portion embedded in the spread-spectrum signal, for detecting, at the respective chip location of each in-phase-header-detection signal and of each quadrature-phase-header-detection signal for each path, 40 each match of the data-chip-sequence signal with the second impulse response, and for outputting, responsive to each detected match, a data-detection signal having an in-phase-data amplitude and a quadrature-phase data amplitude;

45 product means, coupled to an output of said header-matched filter and to an output of said header-timing circuit, for multiplying the in-phase-header amplitude and the quadrature-phase-header amplitude of each header-detection

signal by the in-phase-data amplitude and the quadrature-phase-data amplitude of each data-detection signal, at each  
50 corresponding chip location, respectively, thereby generating the plurality of in-phase-weighted elements and the plurality of quadrature-phase-weighted elements for each data symbol of the data-symbol-sequence signal;

adding means, coupled to an output of said product  
55 means, for adding the plurality of in-phase-weighted elements and the plurality of quadrature-phase-weighted elements for a respective data symbol to generate a sum signal of the respective data symbol;

*17 cont*  
a combiner memory, coupled to an output of said adding  
60 means, for storing the sum signal; and

a data demodulator, coupled to said combiner memory, for detecting data from the sum signal.

12. A multipath-combining method for use with a spread-spectrum receiver for receiving a spread-spectrum signal arriving at different times from a plurality of paths, with the spread-spectrum signal having a plurality of packets with each  
5 packet having a header followed by a data portion, with the header including a header-chip-sequence signal, and with the data portion including a data-symbol-sequence signal, with each data symbol of the data-symbol-sequence signal spread-spectrum processed by a data-chip-sequence signal, said multipath-combining method comprising the steps of:

15 a. detecting, with a first impulse response matched to the header-chip-sequence signal of the header embedded in the spread-spectrum signal, within a packet and for each path, each match of the header-chip-sequence signal with the first impulse response, with a time difference between receiving each path of the spread-spectrum signal greater than a time of each chip of the header-chip-sequence signal;

20 b. outputting, in response to each detected match above a header threshold, a header-detection signal having an in-phase-header amplitude and a quadrature-phase-header amplitude and a respective chip location;

c. storing the in-phase-header amplitude and the quadrature-phase-header amplitude and the respective chip location of each header-detection signal;

25 d. detecting, with a second impulse response matched to the data-chip-sequence signal embedded in the data portion of the spread-spectrum signal, at the respective chip location of each header-detection signal for each path, each match of the data-chip-sequence signal with the second impulse response;

30 e. outputting, responsive to each detected match, a data-detection signal having an in-phase-data amplitude and a quadrature-phase-data amplitude;

f. multiplying the in-phase-header amplitude and the quadrature-phase-header amplitude of each header-detection signal with the in-phase-data amplitude and the quadrature-phase-data amplitude of each data-detection-signal at each

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corresponding chip location, respectively, thereby generating a plurality of in-phase-weighted elements and a plurality of quadrature-phase-weighted elements for each data symbol of the data-symbol-sequence signal; and

g. adding the plurality of in-phase-weighted elements and the plurality of quadrature-phase-weighted elements for a respective data symbol as a sum signal of the respective data symbol.

13. The multipath-combining method as set forth in claim 12, wherein the step of (c) storing includes the step of buffering a plurality of header-detection signals corresponding to the plurality of paths.

14. The multipath-combining method as set forth in claim 12 further including the step of generating a header pattern responsive to each occurrence of the header-detection signal within a frame of the header-chip-sequence signal.

15. The multipath-combining method as set forth in claim 12 further including the step of detecting data from the sum signal.

16. The multipath-combining method as set forth in claim 12 further including the steps of:

h. detecting, from a plurality of header-detection

signals within the packet, a strongest header-detection signal;  
and

i. outputting, responsive to the strongest header-detection signal, a packet-start signal.